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EXAMINER	
MURALIDAR, RICHARD V	
ART UNIT	PAPER NUMBER
2838	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,275	LIPCSEI ET AL.	
	Examiner	Art Unit	
	Richard V. Muralidar	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13 and 16* is/are allowed.

6)☒ Claim(s) *1-10 and 19-23* is/are rejected.

7)☒ Claim(s) *14,15,17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07/08/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6, 19, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Wei [U.S. 2004/0100805].

With respect to claims 1 and 6, [amended] Wei discloses a power converter [Fig. 2, par. 0005 lines 1-5, microprocessor with a power converter], said power converter comprising: a transformer [Fig. 2, transformer M] having a primary winding and a secondary winding [Fig. 2, transformer M with primary winding W1, secondary winding W2]; and a plurality of switches coupled to said primary and secondary winding [Fig. 2 switches Q1-Q6], said plurality of switches responsive to at least one control signal to short said primary and secondary winding during a first reset time interval [Fig. 2 and Fig. 5 show that Q1, Q2, and Q6 operate to short the primary and secondary of transformer M using the hard switching scheme discussed in par. 0041 and 0042; Q1 turns ON to energize the primary winding from power source Vin, Q2 turns ON to short the primary winding to the secondary winding, and Q6 turns ON to form a ground/ return path to power source Vin, which forms a complete short of primary and

secondary windings], said plurality of switches includes a first pair of switches coupled in series to one end of said secondary winding [Fig. 2, the first pair of switches is Q1 and Q2; these are connected in series through primary winding W1 and capacitor C1, and connected to the top end of secondary winding W2] and a second pair of switches coupled in series to an opposite end of said secondary winding [Fig. 2, the second pair of switches is Q3 and Q4, these are connected in series through primary winding W1 and capacitor C1, and connected to the bottom end of secondary winding W2]; and a controller [par. 0026] configured to provide a first [Fig. 5, the first signal is that applied to Q1 and Q2- the first pair of switches] and a second control signal [Fig. 5, the second signal is that applied to Q3 and Q4- the second pair of switches] to said first and second pairs of switches, respectively, wherein said first control signal simultaneously controls said first pair of switches [Fig. 5, Q1 and Q2 are shown being switched simultaneously on and off, in synchronization with each other] and said second control signal simultaneously controls said second pair of switches [Fig. 5, Q3 and Q4 are shown being switched simultaneously on and off, in synchronization with each other] over an entire cycle of said power converter [The switching of the first pair and second pair occur over one full cycle, as shown in Fig. 5. Note- this particular timing corresponds to a hard switching scheme- per par. 0041 and 0042. From Fig. 5, it can be seen that *4 signals are used to operate the 6 switches of the converter*- per applicant's instant invention (applicant's Figs. 2 and 3, and page 4 of the specification). Switches Q1 and Q2 are triggered by a 1st common signal; Q3 and Q4 are triggered

by a 2nd common signal; Q5 is triggered by a 3rd separate signal; and Q6 is triggered by a 4th separate signal].

With respect to claim 19, [amended] Wei discloses a power converter comprising a plurality of DC to DC converters coupled in parallel [page 4 par. 0053; Fig. 8], at least one of said plurality of DC to DC converters [Fig. 8 converters 28, 30, 32, 34] comprising: a transformer [M1] having a primary winding and a secondary winding [W1 and W2]; a plurality of switches coupled to said primary and second winding [switches Q1-Q8], said plurality of switches responsive to at least one control signal to short both said primary and secondary winding during a first reset time interval [Fig. 8 is the plural "multi-output" version of Fig. 2, with multiple, parallel output converters connected to the secondary, therefore the primary and secondary are shorted in the same manner], said plurality of switches includes a first pair of switches coupled in series to one end of said secondary winding [Fig. 2, the first pair of switches is Q1 and Q2] configured to be simultaneously controlled using a first control signal [Fig. 5, switches Q1 and Q2 are shown controlled by the same signal over one full cycle] and a second pair of switches coupled in series to an opposite end of said secondary winding [Fig. 2, switches Q3 and Q4] configured to be simultaneously controlled using a second control signal [Fig. 5, switches Q3 and Q4 are shown controlled by the same signal over one full cycle], wherein the first pair of switches is coupled in series [Fig. 2, switches Q1 and Q2 are coupled in series through primary winding W1 and capacitor C1] to one end of said secondary winding [Fig. 2, switch Q2 is coupled to the top end of secondary winding w2] and the second pair of switches is coupled in series [Fig. 2, switches Q3 and Q4

are coupled in series through primary winding W1 and capacitor C1] to an opposite end of said secondary winging [Fig. 2, switch Q3 is coupled to the bottom end of secondary winding w2]; and a controller [par. 0026] configured to provide a first [Fig. 5, the first signal is that applied to Q1 and Q2- the first pair of switches] and a second [Fig. 5, the second signal is that applied to Q3 and Q4- the second pair of switches] control signal to said first and second pairs of switches, respectively, wherein said first control signal simultaneously controls said first pair of switches and said second control signal simultaneously controls [Fig. 5, Q3 and Q4 are shown being switched simultaneously on and off, in synchronization with each other] said second pair of switches over an entire cycle of said power converter [The switching of the first pair and second pair occur over one full cycle, as shown in Fig. 5. Note- this particular timing corresponds to a hard switching scheme- per par. 0041 and 0042. From Fig. 5, it can be seen that *4 signals are used to operate the 6 switches of the converter*- per applicant's instant invention (applicant's Figs. 2 and 3, and page 4 of the specification). Switches Q1 and Q2 are triggered by a 1st common signal; Q3 and Q4 are triggered by a 2nd common signal; Q5 is triggered by a 3rd separate signal; and Q6 is triggered by a 4th separate signal].

With respect to claim 22, [original] Wei discloses that said plurality of switches for each said DC to DC converter are responsive to control signals from a driver associated with each said DC to DC converter [page 2 par. 0026].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5, 7-10, 20-21, and 23 are rejected under 35 U.S.C. 103(a) as being obvious over Wei [U.S. 2004/0100805].

With respect to claims 2 and 7, [original] Wei discloses that said plurality of switches comprises: a first high side switch [Fig. 2 switch Q1] and a first low side switch [Fig. 2 switch Q3] coupled in series along a first path [Fig. 2 path 22] of a full bridge circuit [Fig. 2 switches Q1-Q4 forms a full bridge], a first node between said first high side switch and said first low side switch [Fig. 2 node 24]; and a second high side switch [Fig. 2 switch Q4] and a second low side switch [Fig. 2 switch Q2] coupled in series along a second path [Fig. 2 path 20] of said full bridge circuit, a second node [Fig. 2 node 24] between said second high side switch and said second low side switch, wherein said primary winding [Fig. 2 primary W1] is coupled between said first node and said second node, *and wherein three switches [Q1, Q2, and Q6] close to short the primary and secondary windings during a reset time interval, in a hard-switching scheme [par. 0041, 0042].* Wei does not disclose that the said first and second high side switches are adapted to open and said first and second low side

switches are adapted to close during said first reset time interval to short said primary winding, in the hard-switching scheme embodiment.

However, Wei teaches a second embodiment called a soft-switching scheme *[shown in Fig. 3]; in which two switches [Q2 and Q3] close to short the primary and secondary together [shown in Fig. 4C], per applicant's language*- wherein said first and second high side switches [Q1 and Q4] are adapted to open and said first and second low side switches [Q2 and Q3] are adapted to close during said first reset time interval to short said primary winding [per the soft switching scheme shown in Fig. 3, Fig. 4C].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the hard-switching scheme [Fig. 2, Fig. 5] with the soft-switching scheme [Fig. 2, Fig. 3] to control the converter shown in Fig. 2 to get the best possible advantages combined into one switching scheme. An advantage of the soft switching scheme is that it allows for efficient power conversion (e.g. 90%) in combination with high voltage conversion ratios [par. 0039], whilst the hard-switching scheme allows for increased voltage-step down capability and reduced switching losses [par. 0041]. Combined advantages would include both of these.

Additionally, the examiner notes that applicant's use of language such as "adapted to" does not constitute a positive limitation in any patentable sense, since such language only requires the switches be capable of performing the intended function, instead of actually doing it *[MPEP 2106 11C]*. The cited switches are clearly capable of shorting the primary and the secondary windings.

With respect to claims 3 and 8, [original] Wei discloses that said plurality of switches further comprises: a first rectifier switch coupled to one end of said secondary winding [Fig. 2 switch Q5]; and a second rectifier switch coupled to an opposite end of said secondary winding [Fig. 2 switch Q6], wherein said first and second rectifier switches are adapted to close during said first reset time interval to short said secondary winding [Fig. 4A and 4C free wheeling mode show the rectifier switches shorting the secondary to ground].

With respect to claims 4 and 9, [original] Wei discloses that said first low side switch [Q2] of said first path of said full bridge circuit and said first rectifier switch [Q5] are responsive to a first control signal and said second low side switch [Q3] of said second path of said full bridge circuit and said second rectifier switch [Q6] are responsive to a second control signal [the configurations in Fig 4C, 7A and 7C show that Q2 and Q5 are synchronized, and Q3 and Q6 are synchronized].

With respect to claims 5 and 10, [original] Wei discloses that said first high side switch [Q4] of said first path of said full bridge circuit is responsive to a third control signal and said second high side switch [Q1] of said second path of said full bridge circuit is responsive to a fourth control signal [Figs. 4A, 4C, 7A and 7C show switches Q4 and Q1 synchronized].

With respect to claim 20, [original] Wei discloses that said plurality of switches comprises: a first high side switch and a first low side switch coupled in series along a first path of a full bridge circuit, a first node between said first high side switch and said first low side switch; and a second high side switch and a second low side switch

coupled in series along a second path of said full bridge circuit, a second node between said second high side switch and said second low side switch, wherein said primary winding is coupled between said first node and said second node, and wherein said first and second high side switches are adapted to open and said first and second low side switches are adapted to close during said first reset time interval to short said primary winding [Fig. 8 is the plural "multi-output" version of Fig. 2, with multiple, parallel output converters connected to the secondary. Therefore the first and second high side switches and first and second low side switches respectively open and close in exactly the same manner as described for Fig. 2 for the previous claims].

With respect to claim 21, [original] Wei discloses that said plurality of switches further comprises: a first rectifier switch coupled to one end of said secondary winding; and a second rectifier switch coupled to an opposite end of said secondary winding, wherein said first and second rectifier switches are adapted to close during said first reset time interval to short said secondary winding [Fig. 8 is the plural version of Fig. 2, with multiple, parallel output converters connected to the secondary. Therefore the first and second rectifier switches close to short the secondary winding in exactly the same manner as described for Fig. 2 for the previous claims].

With respect to claim 23, [original] Wei discloses that said plurality of switches comprise MOSFET transistors [page 2, par. 0026 states Q1-Q6 are FETs; the most popular ones are known to be MOSFETs] and said driver comprises a dual MOSFET driver [page 2, par. 0026, the driving circuit is well known in the art, and the MOSFET driver/ dual driver is widely used to drive MOSFETs].

Allowable Subject Matter

Claims 13 and 16 are allowed. Claims 14, 15, 17, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or suggest either of the rectifier switches being simultaneously controlled with either the first or second pair of switches over an entire cycle, as recited in independent claims 13 and 16.

RESPONSE TO ARGUMENTS

Applicant's filing on 11/13/2006 did not contain any arguments, with the exception of stating that Wei [U.S. 2004/0100805], also currently published as U.S. 6757184, does not meet the claim language as amended. The amended claims have been addressed in the action above. The applicant is encouraged particularly to take note of Wei's use of 4 signals to control 6 switches, as embodied in the *hard-switching scheme*, Fig. 5 and par. 0041 and 0042.

Conclusion

The following reference is cited for its disclosure of a non-isolated bridge buck DC-DC converter with self-driven synchronous rectifiers. Prior art [US2004/0246748A1] by Xu is cited for the disclosure of a similar arrangement of transistors to short-circuit the primary and secondary windings of a transformer to ground.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard V. Muralidar whose telephone number is 571-272-8933. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl D. Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/23/2007
RVM

Adolf Denero Berhane
Primary Examiner